JAN 26 2004

# TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.: INTL-0328-US

In Re Application Of: JOHN S. SADOWSKY

| Serial No. | Filing Date | Examiner | Group Art Unit |
|---|---|---|---|
| 09/670,231 | September 28, 2000 | Mujtaba M. Chaudry | 2133 |

Invention: A DECODER FOR TRELLIS-BASED CHANNEL ENCODING

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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Dated: January 23, 2004

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|---|---|---|---|---|
| Applicant: | JOHN S. SADOWSKY | § | Group Art Unit: | 2133 |
| Serial No.: | 09/670,231 | § | Examiner: | Mujtaba M. Chaudry |
| Filed: | September 28, 2000 | § | | |
| For: | A DECODER FOR TRELLIS-BASED CHANNEL ENCODING | § | Atty. Dkt. No.: | INTL-0328-US (P8031) |

SC #9 2/4/04

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APPEAL BRIEF

Sir:

Applicant respectfully appeals from the final rejection mailed September 2, 2003.

## I. REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 011208/0864.

## II. RELATED APPEALS AND INTERFERENCES

None.

## III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-26. Claims 1-26 are pending. Claims 1-26 are the subject of this appeal.

## IV. STATUS OF AMENDMENTS

All Amendments prior to the Final Office Action have been entered. No amendments have been filed since receipt of the Final Office Action.

## V. SUMMARY OF THE INVENTION

In various embodiments, the present invention includes a system and method for efficiently performing specialized operations, and pertain to the implementation of certain trellis-based algorithms. The algorithm class is used in practice in a number of applications in communications and signal processing, including (but not limited to) coding and decoding convolutional and turbo codes, channel equalization, and speech coding.

In Figure 1, a system 100 includes a digital signal processor 10 and a butterfly coprocessor 28. Digital signal processors, or DSPs, are specialized microprocessors with architectures that are tuned for digital signal processing. DSPs typically feature circuitry that may perform high-speed arithmetic operations, data transfers to and from external devices, and multiple accesses to memories.

In Figure 1, the DSP 10 includes two buses, a memory store bus 22 and a memory load bus 24. The memory store bus 22 and the memory load bus 24 extend beyond the digital signal processor 10, for connecting to a memory 30.

An arithmetic unit 20 is coupled to the memory store bus 22 and the memory load bus 24. The arithmetic unit 20 may include one or more multiply accumulate units, registers, and other circuitry for performing arithmetic operations. Also coupled to the memory store bus 22 and the memory load bus 24 is a data address generator 26. The data address generator 26 identifies the particular location in the memory 30 to be either loaded or stored. The data address generator 26 performs this operation on behalf of other circuitry of the DSP 10, such as the arithmetic unit 20.

In one embodiment, the system 100 further includes a butterfly coprocessor 28. The butterfly coprocessor 28 is not part of the DSP 10, but is coupled to the DSP 10 by the memory store and memory load busses 22 and 24. Like the arithmetic unit 20, the butterfly coprocessor 28 has access to the memory 30 using these busses. In one embodiment, the DSP 10 performs memory management on behalf of the butterfly coprocessor 28, for performing high-speed and parallel butterfly operations. See Specification, pp. 5-6.

In Figure 9, shown is a portion of a trellis diagram, which is a state machine used to describe the behavior of an encoder. The trellis diagram includes stages k, k+1, and k+2. A sliding window 110 encases stage k and k+1. A decoder may use the sliding window 110 to arbitrarily compute the branch metrics 106 along the trellis. See Specification, p. 14.

For example, in stage k, from the node $72_k$ corresponding to the state 00, a branch 74c and a branch 74d extend to nodes $72_{k+1}$ (at stage k+1). Likewise, from the node $72_k$ corresponding to the state 01, two branches 74e and 74f extend. From node $72_k$ (state 10), branches 74g and 74h, and from node $72_k$ (state 11), branches 74i and 74j, extend to the node $72_{k+1}$ (stage k+1). The branches 74c, 74e, 74g and 74i correspond to a "0" input value to the encoder 50 while the branches 74d, 74f, 74h and 74j correspond to the "1" input value.

While the sliding window 110 is in the position in Figure 9, the decoder computes branch metrics 106 for each of the branches 74c through 74j, for a total of eight computations. Except when k=0, one or more paths 82 extend to the nodes $72_k$ from prior stages. One of the paths 82 is the survivor path. Accordingly, a new path metric 108 may be calculated by taking the path metric 108 of the survivor path. A first branch metric 106 may be added to the path metric 108, then a second branch metric 106 may be added to the path metric 108. The two results may be

compared. The path 82 with the larger path metric 108 is the new survivor path for stage k. This group of calculations is known as a butterfly operation.

Once the butterfly operation is complete for stage k, the sliding window 110 may be moved, forward or backward, according to the algorithm, so that the next group of butterfly operations may be performed.

For the sliding window 110 of Figure 9, up to four butterfly operations may be performed, one for each node $72_k$. The branch metric 106 of each branch 74 is added to the path metric 108, (addition operation). Each resulting path metric 108 is then compared to the other path metric 108 to determine which result is the larger (compare operation). The resulting path metric 108, or survivor path, is selected (select operation). The butterfly operation is thus sometimes known as the add-compare-select, or ACS, operation. Finally, the survivor path is stored, such as in a memory. See Specification, pp. 14-15.

In Figure 10, according to one embodiment, a system 200 may be used for performing butterfly operations such as those described above. The system 200 includes one or more butterfly units 202, a branch metric unit 204, and a path metric memory 206. Together, the circuitry of the system 200 may perform the ACS, or log-MAP, butterfly operation.

In the embodiment of Figure 10, each butterfly unit 202 receives a branch metric 106 from the branch metric unit 204. Since there are four nodes 72 in each stage k, four butterfly units 202 are provided. Thus, according to one embodiment, each butterfly unit 202 may perform calculations in parallel with each other butterfly unit 202, so that new path metrics for each state, 00, 01, 10, and 11, may be calculated simultaneously.

Further, each butterfly unit 202 receives a path metric 108 from the path metric memory 206. With this information, the butterfly units 202 may each perform add-select-compare operations for a given node $72_k$ of the trellis diagram.

The output path of each butterfly unit 202 is also coupled to the path metric memory 206. Each butterfly unit 202 may thus send the resulting path metric to the path metric memory 206 for storage, until a new set of butterfly operations, at stage k+1, is performed. See Specification, pp. 15-16.

The butterfly coprocessor 28 thus implements parallel butterfly operations using multiple butterfly units and may accordingly increase the throughput of performing the very complex operations involved in decoding a channel bit stream.

## VI. ISSUES

**A. Are Claims 1-5 and 21 Patentable Under 35 U.S.C. § 102(b) Over Amon?**

**B. Is Claim 6 Patentable Under 35 U.S.C. § 102(b) Over Amon?**

**C. Are Claims 7-9 and 11-12 Patentable Under 35 U.S.C. § 102(b) Over Amon?**

**D. Is Claim 10 Patentable Under 35 U.S.C. § 102(b) Over Amon?**

**E. Is Claim 23 Patentable Under 35 U.S.C. § 102(b) Over Amon?**

**F. Are Claims 25 and 26 Patentable Under 35 U.S.C. § 102(b) Over Amon?**

**G. Are Claims 13-14 and 17-20 Patentable Under 35 U.S.C. § 102(b) Over Amon?**

**H. Is Claim 15 Patentable Under 35 U.S.C. § 103(a) Over Amon In View of Czaja?**

**I. Is Claim 16 Patentable Under 35 U.S.C. § 103(a) Over Amon In View of Czaja?**

**J. Is Claim 22 Patentable Under 35 U.S.C. § 103(a) Over Amon In View of Czaja?**

**K. Is Claim 24 Patentable Under 35 U.S.C. § 103(a) Over Amon In View of Czaja?**

## VII. GROUPING OF THE CLAIMS

For purposes of this appeal, the claims do not stand or fall together. For purposes of this appeal, Applicant has grouped together claims 1-5 and 21; claims 7-9, 11-12; claims 25 and 26; and claims 13-14 and 17-20, as set forth above.

## VIII. ARGUMENT

**A. Claims 1-5 and 21 Are Patentable Under 35 U.S.C. § 102(b) Over Amon**

Claim 1 recites a system including a digital signal processor (DSP) and a butterfly coprocessor connected to the DSP to perform an operation scheduled by the DSP. Claims 1-5 and 21 stand rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,742,621 (Amon). This rejection is improper. Under §102 , it is not enough that a prior art reference discloses all the claimed elements in isolation. Rather, as stated by the Federal Circuit, "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984). Such a showing is entirely lacking here.

With respect to claim 1, Amon does not disclose "a digital signal processor" and "a butterfly coprocessor coupled to the digital signal processor to perform an operation scheduled by the digital signal processor" as recited by claim 1. In this regard, the Examiner states that the digital signal processor of Amon is all of data processing system 20 shown in FIG. 1 of Amon. Final Office Action, p. 4. As such, the program control unit 46 of Amon (contended by the Examiner to be the "butterfly processor") is part of the digital signal processor and is thus not a separate butterfly coprocessor coupled thereto.

More so, the Examiner relies on col. 6, lns. 11-16 of Amon to support the contention that program control unit 46 is a butterfly coprocessor. However, this portion of Amon does not relate to program control unit 46. Instead this portion merely states that a control circuit within arithmetic logic unit (ALU) 54 performs control functions for the ALU in response to instructions received from program control unit 46. Amon, 6:10-16. Thus, to the extent that butterfly operations are performed, they are performed in arithmetic logic unit 54, which is part of the DSP. For this further reason, there is no butterfly coprocessor coupled to a DSP, and certainly there is no such coprocessor to perform an operation scheduled by the DSP. Thus Amon fails to disclose all claimed elements and it certainly does not disclose them as arranged in claim 1.

For at least these reasons, claim 1 and claims 2-5 depending therefrom and independent claim 21 are patentable over Amon, and the rejection should be reversed.

**B. Claim 6 Is Patentable Under 35 U.S.C. § 102(b) Over Amon**

Dependent claim 6, which depends indirectly from claim 1, further recites that an arithmetic unit of the DSP include one or more registers addressable by a data address generator. Claim 6 stands rejected under §102(b) over Amon. This rejection is improper for the reasons set forth above regarding claim 1 (*see* VIII.A).

Dependent claim 6 is further patentable, as nowhere does Amon disclose registers in an arithmetic unit addressable by a data address generator. In this regard, address generation unit 36 of Amon is coupled to address buses 56-59 and is used to provide addressing modes for the DSP. Amon, 4:5-15. Nowhere however does Amon disclose that the address generation unit 36 addresses registers in ALU 54. Thus the rejection of claim 6 should be reversed.

### C. Claims 7-9 and 11-12 Are Patentable Under 35 U.S.C. § 102(b) Over Amon

Claim 7 depends from claim 1 and further recites that the butterfly coprocessor includes a plurality of butterfly units to perform butterfly operations. Claim 7 and claims 8, 9, and 11-12 depending therefrom stand rejected under §102(b) over Amon. This rejection is improper, at least for the reasons discussed above with regard to claim 1 (*see* VIII.A).

Dependent claim 7 is further patentable, as nowhere does Amon disclose a butterfly coprocessor that includes a plurality of butterfly units. In this regard, the operation of Amon cited by the Examiner (col. 6, lns. 55-58) is not performed in program control unit 46 (contended by the Examiner to be a butterfly coprocessor), but rather in ALU 54, a single unit. For this further reason, claim 7 and claims 8-9 and 11-12 depending therefrom are patentable over Amon, and the rejection should be reversed.

### D. Claim 10 Is Patentable Under 35 U.S.C. § 102(b) Over Amon

Claim 10 depends from claim 8 and further recites that the plurality of butterfly units are coupled to perform approximations of logarithmic sum exponential operations at the direction of the DSP. This rejection is improper, at least for the same reasons discussed above regarding claim 7 (*see* VIII.C).

Dependent claim 10 is further patentable, as nowhere does Amon disclose that a plurality of butterfly units performs approximations of logarithmic sum exponential operations, and certainly does not disclose such operations performed at the direction of a DSP. Thus the rejection of claim 10 should be reversed.

### E. Claim 23 Is Patentable Under 35 U.S.C. § 102(b) Over Amon

Dependent claim 23 depends from claim 22, itself dependent from claim 21. For the same reasons discussed in Section VIII.A, claim 23 is patentable. Further, because claim 22 is

not rejected under § 102, the §102 rejection of claim 23 is further improper, and the rejection should be reversed.

**F. Claims 25 and 26 Are Patentable Under 35 U.S.C. § 102(b) Over Amon**

Dependent claims 25 and 26 depend from claim 24, itself dependent from claim 21. For the same reasons discussed in Section VIII.A, these claims are patentable. Further, because claim 24 is not rejected under § 102, the §102 rejection of claims 25 and 26 is further improper and the rejections should be reversed.

**G. Claims 13-14 and 17-20 Are Patentable Under 35 U.S.C. § 102(b) Over Amon**

Claim 13 recites a method including identifying a stage of a trellis diagram; calculating branch metrics for each node of the stage; and simultaneously computing two or more path metrics for the stage based upon the branch metrics. Claims 13-14 and 17-20 stand rejected under 35 U.S.C. §102(b) over Amon. This rejection is improper.

With respect to claim 13, nowhere does Amon disclose "simultaneously computing two or more path metrics for the stage based upon the branch metrics." In this regard, Appellant respectfully disagrees that Amon "teaches simultaneously computing two or more path metrics (PM1 and PM2) based upon the branch metrics (blocks 101-103) in Figure 3...." Final Office Action, p. 3.

Instead, in Amon the path metrics are not simultaneously computed, as the path metrics are computed at different steps and at different times. Amon merely states that a second previous path metric is reloaded into a register while a path metric is determined. This does not disclose simultaneously computing two or more path metrics. For at least this reason, claim 13 and claim 14 depending therefrom and claims 17 and 19, and claims 18 and 20 depending therefrom are patentable over Amon, and the rejection should be reversed.

## H. Claim 15 Is Patentable Under 35 U.S.C. § 103(a) Over Amon In View of Czaja

Claim 15 depends from claim 13 and further recites identifying a number of nodes in a stage; identifying a number of branches extending from each node; and calculating a branch metric for each branch. Claim 15 stands rejected under 35 U.S.C. § 103(a) over Amon in view of U.S. Patent No. 5,796,757 (Czaja). This rejection is improper.

As discussed above (*see* VIII.G), Amon does not teach or suggest simultaneously computing two or more path metrics. Nor does Czaja. Because not all claim limitations are taught or suggested by either reference, a *prima facie* case of obviousness has not been made out. *In re Royka,* 180 U.S.P.Q. 580 (C.C.P.A. 1974). Accordingly, claim 15 is patentable over the proposed combination, and the rejection should be reversed.

## I. Claim 16 Is Patentable Under 35 U.S.C. § 103(a) Over Amon In View of Czaja

Claim 16 depends from claim 14 and further recites, *inter alia*, allocating a butterfly unit for each branch extending from a node of a trellis diagram stage, in which each butterfly unit calculates a new path metric from a prior path metric and a branch metric. Claim 16 stands rejected under §103(a) over Amon in view of Czaja. The rejection is improper, at least for the reasons discussed above regarding claim 15 (*see* VIII.H).

Dependent claim 16 is further patentable, as neither Amon nor Czaja teach or suggest allocating a butterfly unit for each branch extending from a node. In this regard, the portions of ALU 54 recited by the Examiner (Final Office Action, p. 9) do not make up a butterfly unit for each branch. That is, units 92 and 80 of Amon (i.e., barrel shifter and bit field unit 92, and accumulator and rounding unit 80 of FIG. 2) are single units and cannot perform calculations of new path metrics for each branch simultaneously, as only a single such rounding unit and shifter

unit is present in Amon. For this further reason, claim 16 is patentable, and the rejection should be reversed.

**J. Claim 22 Is Patentable Under 35 U.S.C. § 103(a) Over Amon In View of Czaja**

Claim 22 depends from claim 21 and stands rejected under 35 U.S.C. § 103(a) over Amon in view of Czaja. As discussed above regarding claim 21 (*see* VIII.A), from which claim 22 depends, Amon does not teach or suggest a butterfly coprocessor coupled to a digital signal processor to perform an operation scheduled by the digital signal processor. Nor does Czaja. In this regard, the Examiner nowhere asserts that Czaja has such components. Accordingly, claim 22 depending from claim 21 is patentable over the proposed combination, and the rejection should be reversed.

**K. Claim 24 Is Patentable Under 35 U.S.C. § 103(a) Over Amon In View of Czaja**

Dependent claim 24 depends from claim 23 and further recites that the butterfly coprocessor includes a plurality of butterfly units equaling the number of nodes in a stage of a trellis diagram. For the same reasons discussed above regarding claim 22 (*see* VIII.J), claim 24 is patentable. Claim 24 is patentable for the further reason that there are no plurality of butterfly units in either of the proposed references, as discussed above with regard to claim 16 (*see* VIII.I). Thus the rejection of claim 24 should be reversed.

## IX. CONCLUSION

Since the rejections of the claims are baseless, they should be reversed.

Respectfully submitted,

Date: January 23, 2004

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## APPENDIX OF CLAIMS

The claims on appeal are:

1. A system comprising:

a digital signal processor comprising a bus connectable to a memory; and

a butterfly coprocessor coupled to the digital signal processor to perform an operation scheduled by the digital signal processor.

2. The system of claim 1, wherein the digital signal processor further comprises:

a data address generator coupled to the bus to address the memory on behalf of a requesting device.

3. The system of claim 2, wherein the digital signal processor further comprises an arithmetic unit to perform arithmetic operations in the digital signal processor.

4. The system of claim 3, wherein the arithmetic unit further comprises a branch metric unit to perform branch metric calculations.

5. The system of claim 4, wherein the arithmetic unit further comprises one or more registers to which the branch metric unit may store one or more results.

6. The system of claim 5, further comprising one or more registers in the arithmetic unit addressable by the data address generator.

7. The system of claim 1, wherein the butterfly coprocessor further includes a plurality of butterfly units to perform butterfly operations.

8. The system of claim 7, wherein the butterfly operations are parallel operations.

9. The system of claim 8, wherein the plurality of butterfly units in the butterfly coprocessor are coupled to further perform add-compare-select operations at the direction of the digital signal processor.

10. The system of claim 8, wherein the plurality of butterfly units in the butterfly coprocessor are coupled to further perform approximations of logarithmic sum exponential operations at the direction of the digital signal processor.

11. The system of claim 8, wherein the data address generator is coupled to access a path metric retrieved from a path metric memory.

12. The system of claim 11, wherein the data address generator of the digital signal processor is coupled to retrieve a branch metric from the branch metric unit.

13. A method comprising:

identifying a stage of a trellis diagram;

calculating branch metrics for each node of the stage; and

simultaneously computing two or more path metrics for the stage based upon the branch metrics.

14. The method of claim 13, further comprising:

storing the path metrics in a memory.

15. The method of claim 13, calculating the branch metrics for each node of the stage further comprising:

identifying a number of nodes in the stage;

identifying a number of branches extending from each node; and

calculating a branch metric for each branch.

16. The method of claim 14, simultaneously computing two or more path metrics for the stage based upon the branch metrics further comprising:

identifying a node of the stage;

retrieving a prior path metric from the memory, wherein the prior path metric leads to the node;

identifying a number of branches extending from the node in the stage; and

allocating a butterfly unit for each branch extending from the node, wherein the butterfly unit calculates a new path metric from the prior path metric and the branch metric.

17. A method comprising:

receiving a request to decode a bit stream, wherein the bit stream was encoded by an encoder and the encoder is described using a trellis diagram;

identifying a stage of the trellis diagram;

computing branch metrics for all nodes of the stage;

retrieving path metrics for a different stage of the trellis diagram from a memory; and

simultaneously calculating new path metrics for each node of the stage.

18. The method of claim 17, further comprising:

storing the new path metrics for each node of the stage in the memory; and

identifying a new stage of the trellis diagram.

19. An article comprising a medium storing a software program which, when executed, causes a processor-based system to:

identify a stage of a trellis diagram;

calculate branch metrics for each node of the stage; and

simultaneously compute two or more path metrics for the stage based upon the branch metrics.

20. The article of claim 19, further storing a software program which, when executed, causes a processor-based system to store the path metrics in a memory.

21. A system comprising:

a digital signal processor, comprising:

a bus connectable to a memory;

a data address generator and

an arithmetic unit; and

a butterfly coprocessor coupled to the digital signal processor to perform an operation scheduled by the digital signal processor.

22. The system of claim 21, wherein the digital signal processor further comprises a software program which, upon execution, causes the system to:

identify a stage of a trellis diagram;

identify a number of nodes in the stage; and

identify a number of branches extending from each node.

23. The system of claim 22, wherein the butterfly coprocessor further comprises a plurality of butterfly units.

24. The system of claim 23, wherein the number of butterfly units equals the number of nodes in the stage.

25. The system of claim 24, wherein the butterfly coprocessor is coupled to compute path metrics for the stage.

26. The system of claim 25, wherein the butterfly units are coupled to simultaneously compute a path metric for each node of the stage.